Development of Fully Digital Control of Pegasus Power Systems

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## Development of Fully Digital Control of Pegasus Power Systems

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<tr>
<td></td>
<td>TF x 6</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Longer pulse lengths</td>
<td></td>
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Local Helicity Injection (LHI) Provides Robust Non-Solenoidal Startup on the PEGASUS ST

**Plasma Parameters**

- $I_p \leq 0.23$ MA
- $\tau_{shot} \leq 0.025$ s
- $B_T = 0.15$ T
- $A = 1.15$–1.3
- $R = 0.2$–0.45 m
- $a \leq 0.4$ m
- $\kappa = 1.4$–3.7

**Injector Parameters**

- $\Sigma I_{inj} \leq 14$ kA
- $I_{inj} \leq 4$ kA
- $V_{inj} \leq 2.5$ kV
- $N_{inj} \leq 4$
- $A_{inj} = 2$–4 cm$^2$
- $I_{arc} \leq 4$ kA
- $V_{arc} \leq 0.5$ kV

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**Helicity Injectors**

- **LFS System**
- **HFS System**

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C. Pierren, APS-DPP, 2018  
A.T. Rhodes TP11.00107, G.M. Bodner YO5.00004, J.A. Reusch YO5.00003
• Drives a wide range of inductive & resistive loads
• 35 optically isolated H-Bridges
  – 12 IGCT
  – 23 IGBT
• Analog feedback control
• Control signals multiplexed to N H-Bridges
  – ‘Splitter-Combiner’ (S/C)

<table>
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<tr>
<th>Load Types</th>
<th>Operating Voltage</th>
<th>$I_{max}$ [kA]</th>
<th>Controlled Power [MVA]</th>
</tr>
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<tr>
<td>Toroidal Field (TF)</td>
<td>900</td>
<td>24</td>
<td>21.6</td>
</tr>
<tr>
<td>Poloidal Field (PF) (x3)</td>
<td>900</td>
<td>16</td>
<td>14.4</td>
</tr>
<tr>
<td>Radial Coil</td>
<td>900</td>
<td>4</td>
<td>3.6</td>
</tr>
<tr>
<td>Divertor Coil</td>
<td>900</td>
<td>4</td>
<td>3.6</td>
</tr>
<tr>
<td>Ohmic Solenoid</td>
<td>2200</td>
<td>32</td>
<td>70.4</td>
</tr>
<tr>
<td>Injector Arc (x4)</td>
<td>900</td>
<td>4</td>
<td>3.6</td>
</tr>
<tr>
<td>Injector Bias (x2)</td>
<td>2200</td>
<td>12</td>
<td>26.4</td>
</tr>
</tbody>
</table>
Present Analog Control Systems Not Easily Modified/Expanded

- Analog circuits susceptible to noise and comparator drift
- Analog controllers require periodic re-tuning
- Control algorithm changes require circuit modifications
- ‘Splitter’ provides no device protections
- Expansion requires building new circuits
- Ohmic (IGCT) specific protection system requires replacement

C. Pierren, APS-DPP, 2018
FPGA Digital Splitter-Combiner (S/C) and Feedback Controller Expand Pegasus Control Capabilities

• Benefits of Field Programmable Gate Array Technology (FPGA):
  – Programmable control algorithms
  – Expandable with off-the-shelf hardware
  – Improved EMI resilience
  – Increased stability (e.g. no comparator drift)

• S/C Improvements:
  – Additional device-level protections
  – Increased number of controllable H-bridges
  – Continuous fault monitoring
  – Reduced fault response time (25 – 200 ns)

• Regain Ohmic solenoid operations

• Expandable to future Ćuk power supplies

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Improved Device-Level IGCT Protections Enables Resumed Ohmic (OH) Operation

- OH solenoid as a diagnostic tool:
  - LHI coupling to subsequent current drive
  - Taylor limit studies
    - J.D. Weberski TP11.00112

- OH plasma diagnostic baselines:
  - Visual Bremsstrahlung
    - C. Rodriguez TP11.00110
  - Thomson Scattering
  - Magnetics (MHD)
    - N. J. Richner TP11.00111
    - C. E. Schaefer TP11.00113

Previous LHI-to-OH Handoff

An Expanded Poloidal Field Array will Improve Shape & Position Control

- New divertor coil array in upper & lower divertor regions
  - X-point control at 0.3 MA
- Added PF to improve shape & position control
- Initially, coil control will be pre-programmed
- Future control may include active feedback
  - Position control
  - Shape control
Increased Toroidal Field is Critical to the Non-Solenoidal Start-Up Mission

- $B_{TF}$ increasing from 0.15 to 0.6 T
- Supports general start-up research:
  - Determining the scalability of LHI
  - Co-axial helicity injection (CHI)
  - Electron Bernstein Wave (EBW) current drive
- Requires doubling of TF power supplies & control channels
  - Number of H-Bridges from 6 to 12
  - Splitter/Combiner control from 12 to 24
- FPGA simplifies controls expansion

**Projected Toroidal Field Scaling of $I_P$**

$A_{inj} = 16 \text{ cm}^2$, $V_{inj} = 500 \text{ V}$, $I_{inj} = 8 \text{ kA}$, $W_{inj} = 1 \text{ cm}$
Injector Power Supply Topology Change Required for Low Ripple, Programmable $V_{inj}(t)$ Control

- H-Bridge regulation of injectors results in oscillations detrimental to the plasma
  - Typically operate with no active regulation
  - $V_{inj}$ controlled with capacitor bank charge voltage
  - $V_{inj}$ voltage droops during shot

- Ćuk power supplies produce a low ripple output with voltage gain capability
  - Low ripple \(\rightarrow\) active $V_{inj}$ regulation during shot
  - Voltage gain \(\rightarrow\) voltage droop compensation
  - Voltage gain \(\rightarrow\) improved energy storage utilization

Example of Regulation Induced Oscillations
FPGA S/C Improves Device-Level Protections

• Splitter Functionality Retained:
  – Multiplexing of command signals to N bridges

• Combiner Functionality Retained:
  – Device-level interpretation of IGBT/IGCT status signals
  – Aggregation of bridge status signals to single assertion of “Coil Set OK”
  – Fault assertion for SCRAM system
  – Identification of faulted device

• FPGA Enabled Improvements:
  – Continuous monitoring of device status
  – State filtering for invalid PWM commands
  – Improved fault response time (25-200 ns)
  – Improved device protections

State-Diagram of Allowed H-Bridge States & Transitions

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FPGA S/C Implementation Leverages Inherent Parallelism of LabVIEW & FPGAs for Asynchronous Operation

Initialization

Q Signal Input

Input State Filter

Splitters

Command Signal Output

Global Variable
State Manager

Status Signal Input

Combiners (IGBT, IGCT)

State Filter Fault Encoder

Bridge Set Monitor (1 of N)

PXI Bus Input

PXI Fault Bus Monitor

Fault Processor

PXI Bus Output

PXI Reset Bus Monitor

SCRAM Assert Output

User Interface Processor

Note: all blocks operate asynchronously

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FPGA S/C Functionality Verified with Custom Testing Platform Prior to Deployment

- Test platform sourced arbitrary optical command signals to challenge the logic of the S/C Under Test (SCUT)
- Required 33 unique challenges
- Challenge results and fault response times reported to User
- Verified all S/C fault responses:
  - IGBT & IGCT status faults
  - Invalid state encoding
  - Invalid state transition command
  - Insufficient state dwell time
  - Valid transit of state diagram → No fault

Test Platform

Present Power Supply Configuration

<table>
<thead>
<tr>
<th>Load</th>
<th>Typ. V</th>
<th>$I_{max}$ [kA]</th>
<th># of Bridges</th>
<th>Bridge Type</th>
<th>S [MVA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TF</td>
<td>900</td>
<td>24</td>
<td>6</td>
<td>2Q</td>
<td>21.6</td>
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<tr>
<td>PF 23</td>
<td>900</td>
<td>16</td>
<td>4</td>
<td>2Q</td>
<td>14.4</td>
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<tr>
<td>PF 67</td>
<td>900</td>
<td>16</td>
<td>4</td>
<td>2Q</td>
<td>14.4</td>
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<tr>
<td>PF 45</td>
<td>900</td>
<td>8</td>
<td>2</td>
<td>4Q</td>
<td>7.2</td>
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<tr>
<td>Radial Coil</td>
<td>900</td>
<td>4</td>
<td>1</td>
<td>2Q</td>
<td>3.6</td>
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<tr>
<td>Divertor Coil</td>
<td>900</td>
<td>4</td>
<td>1</td>
<td>2Q</td>
<td>3.6</td>
</tr>
<tr>
<td>Ohmic Solenoid</td>
<td>2200</td>
<td>32</td>
<td>8</td>
<td>4Q</td>
<td>70.4</td>
</tr>
<tr>
<td>Injector Arc</td>
<td>900</td>
<td>4</td>
<td>1</td>
<td>4Q</td>
<td>3.6</td>
</tr>
<tr>
<td>Injector Bias</td>
<td>2200</td>
<td>12</td>
<td>3</td>
<td>1Q</td>
<td>26.4</td>
</tr>
</tbody>
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Example of Increased Protections and Circuit Schematics of H-Bridge States

H-Bridge Quadrant Voltages [V]

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Q1+</th>
<th>Q1-</th>
<th>Q3+</th>
<th>Q3-</th>
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<tbody>
<tr>
<td>1200</td>
<td></td>
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<td>1100</td>
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<td>800</td>
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<td>700</td>
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<td>600</td>
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<td>500</td>
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<td>400</td>
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<td>300</td>
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<td>200</td>
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<td>100</td>
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<tr>
<td>0</td>
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Enforcement Period

- 16 μs
- 2 μs

Gate Off @ 20 ms

Shot 102364

(1) 4Q Positive Drive

(2) 4Q Positive Regen
Pulse Width Modulation (PWM) is a Voltage Control Technique Commonly Deployed In Power Systems

• Ratio of device (switch) On-time to Off-time known as the Duty cycle

• The output voltage is related to the input voltage through the duty cycle ($D$):

$$\text{H-Bridge} \quad \text{Čuk}$$

$$V_{out} = D \times V_{in} \quad V_{out} = -\frac{D}{1-D} \times V_{in}$$

• Modulating the pulse width or duty cycle provides a means to control the output voltage

• FPGA controller will use PWM where the duty cycle or plant variable, $u(t)$, is generated by a Proportional-Integral-Differential (PID) controller:

$$u(t) = K_P e(t) + K_I \int_0^t e(\tau) d\tau + K_D \frac{de(t)}{dt}$$

$$V_{out} = D \times V_{in} \quad V_{out} = -D \times V_{in}$$

Example of 5 V H-Bridge PWM


FPGA PWM Will Use a Multitiered Architecture: Windows Host ↔ RT Host ↔ Target

- **Windows Host:**
  - User interface (PWM settings, system status, etc.)
  - Main Control Code interface

- **RT Host:**
  - Between shots:
    - Update PWM settings from Windows Host
    - Write shot data to main data server
  - During shot:
    - Receive feedback signal, \( y(t) \), and generate demand signal \( r(t) \)
    - Calculate error signal \( e(t) = r(t) - y(t) \)
    - Calculate plant signal, \( u(t) \), from \( e(t) \)
    - Transmit plant signal to Target

- **FPGA Target:**
  - Measure feedback signal, \( y(t) \) & transmit to RT
  - Receive plant signal, \( u(t) \), from RT (signed duty cycle)
  - Use plant signal to decide on next action
    - State & duration of next PWM cycle

**Communication Mechanisms**
- TCP/IP
- DMA FIFO
- PXI Bus
- VHDCI

Windows Host PC

LabVIEW VI

Real-Time (RT) Controller

LabVIEW Real-time VI

FPGA Hardware

LabVIEW FPGA

Hardware I/O Interface(s)

FPGA Hardware

LabVIEW FPGA

Hardware I/O Interface(s)
FPGA PWM Control Logic to be Verified with Coupled Simulation of LabVIEW FPGA Controller VI and Multisim Circuit Model

- LabVIEW simulation of PWM control signal (plant signal) generation
- Multisim simulation of circuit response (plant response) to control signals
- Data passed between simulation environments each time step

\[ u(t) \]

\[ y(t) \]


C. Pierren, APS-DPP, 2018
Optically Transmitted Local Shunt Voltage Measurement in Development for FPGA PWM Feedback Signal

- Current measured with series shunt resistor: \( I = \frac{V}{R} \)

- Shunt voltage locally converted to 1 bit stream with Sigma-Delta ADC
  - Voltage encoded in the duty cycle of the bit stream

- Bit stream transmitted \textit{optically} to FPGA

- FPGA filters bitstream to recover analog signal

- Benefits include:
  - Linear response
  - Ability to measure DC current
  - Improved signal to noise ratio
  - No integration required
Single Ćuk Module Achieved ~25 ms Flat-Top at ~1.2 MW While Utilizing 60% of the Stored Energy*

- Goal for future injector power supply is a low ripple Ćuk module at 400V & 4kA

- Test results of an Eagle Harbor Technologies Ćuk module:
  - 340 V, 3.4 kA into 100 mΩ load
  - 60% stored energy used (40% to load)
  - No droop in $V_{\text{out}}$ with 100 V droop in $V_{\text{bank}}$
  - 3% peak-to-peak ripple
  - Low frequency ripple can be designed away

*In collaboration with A. Henson, Eagle Harbor Technologies, TP11.00126
Modular Ćuk Power Supply Design Enables Parallel & Series Topologies for Varying Voltages & Currents

Single Module:
400 V & 4 kA

Two Parallel Modules:
400 V & 8 kA

Two Series Modules:
800 V & 4 kA

C. Pierren, APS-DPP, 2018
Development & Deployment Plan for Power Supply & Control System Upgrades

Near-Term

• Complete FPGA SC deployment
  – Improves device protections
  – Enables OH experiments

• FPGA digital PWM
  – Programmable coil & LHI control
  – Advanced control algorithms
    • Combined feedforward & PID control

• DNB power supply & control

• Ćuk converter for injector Arc and Bias power supplies
  – Low ripple, programmable voltage control of helicity injection

Longer-Term

• Active control of helicity injection

• Active injector gas control for injector impedance control

• FPGA replacement of CAMAC timing modules

• RF/EBW power supply & control
Summary of Physics Studies and Experimental Improvements Enabled by Planned & Proposed Upgrades

- Improved device protections enable OH Experiments:
  - Impurity studies
  - Taylor limit studies
  - LHI to OH handoff

- $V_{INJ}(t)$ helicity injection control:
  - Improved helicity drive scans for model validation
  - Active control for improved $I_P(t)$ evolution

- Increased TF:
  - Exploration of higher TF operating space relevant to start-up on larger machines
  - Increased Taylor limit studies
  - CHI, EBW

- PF Expansion:
  - Improved divertor control
  - Improved shape & position control
  - Better coupling to helicity injectors

- DNB Control:
  - Plasma kinetic & impurity measurements
    - $\vec{B}(R,t), J(R,t), T_i(R,t), n_e(R,t), n_Z(R,t)$

- RF/EBW Control:
  - Electron heating
  - Current drive
Physics Studies to be Enabled by Control Upgrades
Improved Device Protections from Initial FPGA SC Deployment
Progress Towards a Digital FPGA PWM Controller
Planned Upgrades to Control System & Power Supplies
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