Enhanced Control for Local Helicity Injection on the Pegasus ST

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**Background**

- Pegasus/LHI Overview
- Power Supply Overview
- Present Control Systems Limitations
- FPGA Upgrade

**Hardware**

- What’s an FPGA?
- NI FPGA System Architecture
- Hardware on Pegasus
- Near-Term FPGA Implementation

**Splitter Combiner**

- S/C Overview
- FPGA S/C Block Diagram
- I/O Requirements
- State Filtering & State Diagram

**Code Testing**

- Overview of FPGA Application Testing
- FPGA Noise Immunity Testing
- Bridge Level Protection Logic Validated
- FPGA S/C BenchTesting

**Future Work**

- Near-Term Work
- Possible Near-Term Physics Studies
- Future Power System Control
- Future FPGA Enabled Physics Studies

**Power Supply**

- Overview of Power Supply Testing

**Future Work**

- Possible Future Work
- Future FPGA Enabled Physics Studies

**Panel size:** 8’ x 4’
Local Helicity Injection (LHI) Provides Robust Non-Solenoidal Startup on the PEGASUS ST

Plasma Parameters
- $I_p \leq 0.23$ MA
- $\tau_{\text{shot}} \leq 0.025$ s
- $B_T = 0.15$ T
- $A = 1.15$–1.3
- $R = 0.2$–0.45 m
- $a \leq 0.4$ m
- $\kappa = 1.4$–3.7

Injector Parameters
- $\sum I_{\text{inj}} \leq 14$ kA
- $I_{\text{inj}} \leq 4$ kA
- $V_{\text{inj}} \leq 2.5$ kV
- $N_{\text{inj}} \leq 4$
- $A_{\text{inj}} = 2$–4 cm²
- $I_{\text{arc}} \leq 4$ kA
- $V_{\text{arc}} \leq 0.5$ kV

C. Pierren, APS-DPP, 2017
Pegasus Driven by ~ 250 MVA Modular Power System

- Drive wide range of loads
- 35 optically isolated H-Bridges
  - 12 IGCT
  - 23 IGBT
- Analog feedback control
- Control signals multiplexed to N bridges
  - ‘Splitter-Combiner’ (S/C)

<table>
<thead>
<tr>
<th>Load Types</th>
<th>Operating Voltage</th>
<th>$I_{max}$ [kA]</th>
<th>Controlled Power [MVA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Toroidal Field (TF)</td>
<td>900</td>
<td>24</td>
<td>21.6</td>
</tr>
<tr>
<td>Poloidal Field (PF) (x3)</td>
<td>900</td>
<td>16</td>
<td>14.4</td>
</tr>
<tr>
<td>Radial Coil</td>
<td>900</td>
<td>4</td>
<td>3.6</td>
</tr>
<tr>
<td>Divertor Coil</td>
<td>900</td>
<td>4</td>
<td>3.6</td>
</tr>
<tr>
<td>Ohmic Solenoid</td>
<td>2200</td>
<td>32</td>
<td>70.4</td>
</tr>
<tr>
<td>Injector Arc (x4)</td>
<td>900</td>
<td>4</td>
<td>3.6</td>
</tr>
<tr>
<td>Injector Bias (x2)</td>
<td>2200</td>
<td>12</td>
<td>26.4</td>
</tr>
</tbody>
</table>

C. Pierren, APS-DPP, 2017
Next Generation LHI Enabled by Planned Power Supply and Control System Upgrades

- FPGA ‘Splitter-Combiner’
  - Expands number of simultaneously controllable bridges
  - Improve IGCT Protections

- Ćuk Converter Power Supply for Injector Arc & Bias
  - Low ripple programmable voltage control

- FPGA Digital Feedback Controllers
  - Programmable coil set and helicity injection control

- Increase TF (H-Bridge)
  - Increased Taylor Limit, confinement studies

- Expand PF (H-Bridge)
  - Improved position and shaping control

Ćuk Converter (Planned)

H-Bridge Topology (1 of 35)

C. Pierren, APS-DPP, 2017
FPGA Digital Splitter-Combiner (S/C) and Feedback Controller Expand Pegasus Control Capabilities

**Benefits of FPGA:**
- Programmable control algorithms
- Expandable with off-the-shelf hardware
- Improved EMI resilience
- Increased stability (e.g. no comparator drift)

**S/C Improvements:**
- Additional device-level protections
- Reduced fault response time
- Continuous fault monitoring

C. Pierren, APS-DPP, 2017
Field Programmable Gate Array (FPGA) Technology Overview

- “Programmable hardware” via low-level logic descriptor languages (VHDL) or high-level (LabVIEW FPGA)

- Input / output interfaces
  - Analog and Digital I/O

- Clocks / timers
  - 10, 40 MHz fundamental

- Direct Memory Access (DMA) interfaces
  - FPGA↔Realtime PC data exchange

- PCI, PXI bus interfaces
  - Inter-FPGA signaling, data exchange, timing

FPGA Resource Types

Source: NI.com, Introduction to LabVIEW Real-Time and FPGA

C. Pierren, APS-DPP, 2017
National Instruments Labview FPGA Platform Provides Flexible Control System Architecture

- **Software Hierarchy**
  - LabVIEW
    - General-purpose language, no timing guarantees
  - LabVIEW Real-time
    - ~100s kHz – class timing guarantees
    - Can act as data processor and pass-through for FPGAs
  - LabVIEW FPGA bit file

- **Hardware Hierarchy**
  - Windows PC
  - Real-time PXI controller
    - Real-time OS, embedded hardware control interfaces
  - FPGA Modules
  - Plant I/O Interface

- **Applications can have varying levels of complexity**
  - FPGA only
  - Multiple FPGAs (and PXI intra-FPGA signaling)
  - FPGA(s) + RT host
  - FPGA(s) + RT host(s) + Windows host

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C. Pierren, APS-DPP, 2017
**FPGA Hardware Employed for Pegasus System**

- **NI PXI 7852R “Hybrid” FPGA (x2)**
  - 8 AI, 8 AO
  - 96 DIO

- **NI PXI 7813R “Digital” FPGA (x1)**
  - 160 DIO channels

- **PXIe-1062Q Crate (x2)**
  - Houses embedded controller (PXIe-8133 / PXIe-8135) and FPGA units
  - Real-time LabVIEW control capability
  - TCP/IP remote control capability

- **Electro Standards Laboratory (ESL) Custom TTL↔Optical Transceiver (x7)**
  - Convert 20 TTL I/O pairs to 20 Optical TX/RX pairs
  - Optical signaling compatible with IGBTs & IGCTs

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*C. Pierren, APS-DPP, 2017*
FPGA Splitter-Combiner Chosen as First Application

- Addresses technical requirements for many applications:
  - Fundamental for planned upgrades

- Improvements enabled by FPGA S/C:
  - Continuous fault monitoring
  - Improved fault response time
  - More robust device protection
  - Increased number of controllable bridges

C. Pierren, APS-DPP, 2017
FPGA Splitter/Combiner Improves Device-Level Protections

• Splitter Functionality Retained:
  – Multiplexing of command signals to N bridges

• Combiner Functionality Retained:
  – Device-level interpretation of IGBT/IGCT status signal
  – Aggregation of bridge status signals to single assertion of “Coil Set OK”
  – Fault assertion for SCRAM system
  – Identification of faulted device

• FPGA Enabled Improvements:
  – Continuous monitoring of device status
  – Protection from invalid PWM commands (state filter)
  – Improved fault response time (25-100 ns)
FPGA Splitter-Combiner Block Diagram

Note: all blocks operate asynchronously

C. Pierren, APS-DPP, 2017
Input/Output Requirements Satisfied by Multi-FPGA System

Present Power Supply Configuration

<table>
<thead>
<tr>
<th>Load</th>
<th>Typ. V</th>
<th>$I_{max}$ [kA]</th>
<th># of Bridges</th>
<th>Bridge Type</th>
<th>Power S [MVA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TF</td>
<td>900</td>
<td>24</td>
<td>6</td>
<td>2Q</td>
<td>21.6</td>
</tr>
<tr>
<td>PF 23</td>
<td>900</td>
<td>16</td>
<td>4</td>
<td>2Q</td>
<td>14.4</td>
</tr>
<tr>
<td>PF 67</td>
<td>900</td>
<td>16</td>
<td>4</td>
<td>2Q</td>
<td>14.4</td>
</tr>
<tr>
<td>PF 45</td>
<td>900</td>
<td>8</td>
<td>2</td>
<td>4Q</td>
<td>7.2</td>
</tr>
<tr>
<td>Radial Coil</td>
<td>900</td>
<td>4</td>
<td>1</td>
<td>2Q</td>
<td>3.6</td>
</tr>
<tr>
<td>Divertor Coil</td>
<td>900</td>
<td>4</td>
<td>1</td>
<td>2Q</td>
<td>3.6</td>
</tr>
<tr>
<td>Ohmic Solenoid</td>
<td>2200</td>
<td>32</td>
<td>8</td>
<td>4Q</td>
<td>70.4</td>
</tr>
<tr>
<td>Injector Arc</td>
<td>900</td>
<td>4</td>
<td>1</td>
<td>4Q</td>
<td>3.6</td>
</tr>
<tr>
<td>Injector Bias</td>
<td>2200</td>
<td>12</td>
<td>3</td>
<td>1Q</td>
<td>26.4</td>
</tr>
</tbody>
</table>

- 3 FPGAs meet I/O needs
- Intra-FPGA communicates via fast PXI bus

<table>
<thead>
<tr>
<th>Optical In</th>
<th>Optical Out</th>
<th>DIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Status IN</td>
<td>93</td>
<td>93</td>
</tr>
<tr>
<td>PWM Commands</td>
<td>27</td>
<td>27</td>
</tr>
<tr>
<td>Command OUT</td>
<td>-</td>
<td>93</td>
</tr>
<tr>
<td>Aggregate Fault</td>
<td>-</td>
<td>11</td>
</tr>
<tr>
<td>SCRAM</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>TOTAL</td>
<td>120</td>
<td>105</td>
</tr>
<tr>
<td>AVAILABLE</td>
<td>160</td>
<td>160</td>
</tr>
</tbody>
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FPGA Enabled State Filtering Increases Device-Level Protections

Configuration of 4Q Bridge in State A

- State navigation controlled by PWM
- S/C filters PWM commands; only valid commands sent to bridges
- Enforces minimum dwell times during operation & fault handling

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Functionality of Custom Electro Standards Laboratory (ESL) Transceivers Verified

- Critical for optical interfacing
- FPGA used to verify ESL Transceiver
  - Test waveforms, clock / pulse generators, etc.
  - 23 VIs developed for transceiver interfacing
  - Interface library also applied to S/C
- Result: Pegasus requirements satisfied

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<table>
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<th>Spec Verified</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>Physical I/O Mapping</td>
<td>TTL ↔ Optical TX/RX</td>
</tr>
<tr>
<td>Optical Power</td>
<td>Signal above threshold</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>Verify data bit rate 10Mbps</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>Quantify susceptibility (none)</td>
</tr>
<tr>
<td>Noise susceptibility</td>
<td>Test EMI resilience (robust)</td>
</tr>
</tbody>
</table>

Pinout Verification VI: TX State Toggled by User

Seven ESL 6760 Units Under Test
Noise Immunity Testing Indicates Optical Interface Improves EMI Resilience

- FPGA system deployed in same environment as present control system
  - Monitored for noise induced state changes every 25 ns

- Tested during operational period with uncharacteristically high levels of noise
  - Present system experienced 4 faults that halted operations
  - FPGA system did not fault: robust to this environment

- Noise resilience should improve reliability and increase run time
State Detection and Transition Filter Logic Verified with Custom Labview FPGA Test Platform

- Core logic implemented:
  - Detect current state of H-bridge
  - Filter states; only valid states, transitions sent to bridges

- Tested with external test platform:
  - Challenged all possible states
  - Challenged all possible state transitions
  - Recorded inferred states and transition validities
  - Compared to design specifications

- Implementation passed hardware proof

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FPGA S/C Functionality to be Verified by Full System Testing Platform Before Deployment

- Created test platform to source arbitrary optical signals:
  - FPGA Target generates user programmed ‘PWM’ and ‘Status’ signals for FPGA Under Test
  - Real Time Host interfaces between User and FPGA Target
  - Target monitors PXI Bus for challenge induced faults
  - Challenge results reported to user

- Mechanics of test bench verified:
  - Proof of concept test
  - Enables automation of S/C testing

- Challenge sequences to verify S/C fault response:
  - IGBT & IGCT status faults
  - Invalid state encoding
  - Invalid state transition command
  - Insufficient state dwell time
  - Valid transit of state diagram → No fault

C. Pierren, APS-DPP, 2017
# Development & Deployment Plan for Power Supply & Control System Upgrades

## Near-Term

- **FPGA Splitter/Combiner**
  - Expands control channels; TF upgrade
  - IGCT protection

- **Ćuk converter for injector Arc and Bias supplies**
  - Low ripple voltage control

- **FPGA digital PWM**
  - Programmable coil & LHI control
  - Advanced control algorithms

## Proposed

- **DNB power supply & control**
- **RF/EBW power supply & control**
- **FPGA replacement of CAMAC timing modules**
Physics Studies Enabled by Planned & Proposed Upgrades

• Helicity Injection Control:
  – Helicity drive scans
  – Potential for tandem operation of low-field and high-field side helicity injection

• Increased TF:
  – Explore higher TF operating space relevant to start-up on larger machines
  – Increased Taylor limit studies

• PF Expansion:
  – Improved vertical position control
  – Better coupling to helicity injectors

• OH Operations:
  – Impurity studies
  – Taylor limit studies
  – LHI to OH handoff

• DNB Control:

• RF/EBW Control:
  – Electron heating
  – Current drive
• FPGAs improve control and support expansion of Pegasus power supply
  – Commercial off-the-shelf hardware and software

• FPGA S/C system designed as first application
  – Protects all power supplies and enables expansion
  – Improves fault response and monitoring
  – Improves device-level protections

• Hardware & design verification in progress prior to powered testing

• Next steps:
  – Ćuk power supplies: Injector Arc & Bias
  – FPGA Digital Control
  – DNB, RF/EBW power supply
Pegasus Power Systems
FPGA Hardware Provides Flexible Control
Hardware & Software Verification
Planned Upgrades to Control System & Power Supplies
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